Novoptel

Application note 6 Firmware Update using XILINX Impact

Revision history

Version	Date	Remarks	Author
0.9.0	02.08.2016	Draft version	B. Koch
0.9.1	26.06.2021	Digilent programmer added	R. Noe
0.9.2	06.07.2021	SPI flash memory added	R. Noe
0.9.3	05.06.2024	Xilinx Vivado added	B. Koch

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Summary

This document describes the firmware update of Novoptel instruments using XILINX Platform Cable USB II, or Digilent HTAG-HS2 rev. A, and XILINX Impact.

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1. Connect the XILINX programmer to the PC



Fig. 1: XILINX Platform Cable USB II

Use a USB cable to connect the programmer box to the PC. Windows should automatically detect the hardware and install the driver.

2. Verify the XILINX cable driver

If the driver is installed correctly, the LED on the programmer box will glow in orange color. The programmer device should appear in the Windows device manager.



Fig. 2: Windows device manager

The driver version can be verified in the device properties.

3. Connect the XILINX programmer to the Novoptel device

Use the flat ribbon cable to connect the XILINX programmer to the JTAG socket at the rear side of the Novoptel device. Power the Novoptel device. If the connection is correct, the LED on the programmer box will glow in color green as soon as the Novoptel device is powered.

4. Open XILINX Impact

If the programmer box is connected to a powered Novoptel device, XILINX Impact should be able to automatically detect the programmer.

B Cable Communication Setup

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Fig. 3: Cable setup in XILINX Impact

Create a new project in XILINX Impact. If the programmer is not detected by XILINX Impact, check the configuration setup by opening the "Cable Setup..." in the menu bar. If the programmer is detected, Impact should automatically initialize the JTAG chain. If not, select "File"->"Initialize Chain" in the menu bar.

If the programmer box is connected to a powered Novoptel device, XILINX Impact should be able to automatically detect the programmer.

5. Program device

5.1 JTAG chain with FPGA and flash memory

Most Novoptel devices until about 2017 contained a JTAG chain with FPGA and flash memory. This is discussed here.



Fig. 4: Correct JTAG chain in XILINX Impact

If the JTAG chain is initialized correctly, two devices should be accessible. An FPGA (e.g. xc6sxl100) and a flash memory (e.g. xcf32p). The FPGA can be programmed using a .bit file to test new firmwares



without overwriting the old one until you cycle the power. The flash memory can be programmed with a .mcs file to permanently upgrade the firmware. The .bit and .mcs files are provided by Novoptel upon request. Right-click on a device and select "Assign New Configuration File..." to assign a file.

legol y		
Boundary-Scan Device 1 (FPGA xc6slx100)	Property Name	Value
Device 2 (PROM2 xcf32p)	Verify	
	General CPLD And PROM Properties	
	Design-Specific Erase Before Programming	V
	Read Protect	
	PROM/CoolRunner-II Usercode (8 Hex Digits)	
	PROM Specific Properties	
	Load FPGA	V
	Parallel Mode	
	Advanced PROM Programming Properties	
	During Configuration: PROM is Configuration Master	
	[select clock source]	External Clock 🔍
	During Configuration: PROM is Slave (clocked extern	

Fig. 5: Programming properties

Before programming the .mcs file, verify the programming properties. Right-click on the flash memory and select "Set Programming Properties...". It is important that the menu item "Design-Specific Erase Before Programming" is activated, see Fig. 5. Finally the programming is started by right-clicking the device and selecting "Program".

5.2 JTAG with FPGA and attached SPI flash memory

Most Novoptel devices since about 2018 contain a JTAG chain with only an FPGA that has attached flash memory. This is discussed here. Example is a PM1000 built in 2021 and to be updated to firmware "polarimeter88_v1070_r137".

Before you can program such a device, one environment variable must be set. In Windows 10:

- Click Windows Logo or Search and type "env".
- Select "Edit the system environment variables".
- The window "System Properties" appears.
- At the bottom click "Environment Variables ...".
- Press "New ..." and define/edit the variable "XIL_IMPACT_SKIPIDCODECHECK" with the value "1".

Edit User Variable		×
Variable name:	XIL_IMPACT_SKIPIDCODECHECK	
Variable value:	1	
Browse Directory.	Browse File	OK Cancel

Fig. 6: Editing environment variable

- Press "OK" to close each window.

Then:

- Launch XILINX Impact.
- Select "Boundary scan".
- Double-click "Boundary scan".

- Right-click to "Initialize chain". After "Identify Succeeded", in this example XC6SLX150, you may close the pop-up window "Device Programming Properties".

- Right-click the FPGA (is or gets green) to "Assign New Configuration File ...".

- Assign the firmware bitfile, here "polarimeter88_v1070_r137.bit". We propose you first test this bitfile. So, for the time being, you say "No" to "Assign SPI or BPI PROM".

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				Right click to Ad
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				Add Non-Allinx Device Ctri+
				Initialize Chain Ctrl+
				Cable Auto Connect Boundary Sc Cable Setup
Console		++	□ & ×	Console Output File Type
Welcome to iMPACT			^	// *** BATCH CMD : setMode -bs
iMPACT Version: 14.7				// *** BATCH CMD : setMode -bs
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Console 🗵 Errors 🔬 Warnings				Console C Errors A Warnings
		ΓΓΓ	Г Г .	No Cable Connection No File Open
Fig. 7: Boundary scan, initialize chain				



Fig. 8: Assign configuration file

- Right-click the FPGA (gets green) to "Program". "Cancel" the pop-up window "Device Programming Properties". After a while (here: 12 s) you see "Program Succeeded". You can test now the firmware on the FPGA. But if you switch off the device and power on again, the old .mcs file will automatically be loaded as firmware from the SPI flash memory into the FPGA.

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Confi	guration Platform Cable USB	II 6 MHz u	usb-hs	Configuration Platform Cable USB II 6 MHz usb-hs

Fig. 9: Program FPGA

If the firmware works satisfactorily you should program it permanently into the SPI flash memory (which takes much longer):

- Right-click the FPGA to "Assign SPI/BPI flash...", here "polarimeter88_v1070_r137.mcs".
- To "Select Attached SPI/BPI", select Data Width "4" for an "SPI PROM", here "S25FL128S". Click OK.



Fig. 10: Assign SPI flash memory file and device

- The attached flash memory is now shown. Right-click to "Set Erase Properties...". In the next window, click "Device 1 (Attached FLASH S25FL128S)" and set the property "Erase" to the value "Full Chip Erase" (not "Device-Specific Erase"). Then click "OK".

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+ □ ♂ × Right click device to select operation Tol CASH X X X X Construction X X Construction X	m5					
Add Xilinx Device Add Non-Xilinx Device Initialize Chain Cable Auto Connect	Ctrl+D Ctrl+K Ctrl+I		Erase / Blank Check Properties - Device 1 Erase P Category Boundary-Scan Device 1 (FPGA xc6skr150)	roperties Property Name	Value	×
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rs 🔬 Warnings Configuration Platform Cable USB II	6 MHz	usb-hs		OK	Cancel Apply	Help
Fig. 11: Set erase proper	ties					

- The flash memory is now shown. Right-click the "FLASH" to "Erase". After some time (here: 93 s) you see "Erase Succeeded".

- Right-click to "Set Programming Properties...". In the next window, click "Device 1 (Attached FLASH S25FL128S)" and uncheck the (initially checked) property "Design-Specific Erase Before Programming". Then click "OK".

- Right-click the flash memory "FLASH" to "Program" it. After some time (here: 379 s) you see "Programming Succeeded". You may close all windows. Upon power-up this .mcs file will be loaded into the FPGA.









6. Usage of Digilent HTAG-HS2 rev. A programmer

The Digilent HTAG-HS2 rev. A Programming Cable for Xilinx® FPGAs (instead of XILINX Platform Cable USB II) can also be used together with XILINX Impact.

Digilent provides a plugin for their programmers with the Xilinx software:

<u>https://reference.digilentinc.com/lib/exe/fetch.php?tok=0cf116&media=http%3A%2F%2Ffiles.digilent.co</u> <u>m%2FSoftware%2FDigilent_Plugin%2FlibCseDigilent_2.5.2-x86-x64-Windows.zip</u> from page

https://reference.digilentinc.com/reference/software/digilent-plugin-xilinx-tools/start

Quoting from a Digilent manual:

The Digilent Plug-in can be installed in the ISE installation directory by copying libCseDigilent.dll (libCseDigilent.so on Linux systems) and libCseDigilent.xml to the plugins directory. For the Windows version of ISE Design Suite, the typical location is

C:\Xilinx\14.1\ISE_DS\ISE\lib\nt\plugins\Digilent\libCseDigilent. For 64-bit Windows, use nt64 in place of nt.

After this procedure, XILINX Impact should be able to recognize FPGA and memory through the Digilent programmer.

7. Firmware Update with XILINX Vivado

Later Novoptel instruments may contain a XILINX Series 7 FPGA such as Artix. In this case XILINX Vivado is required instead of Impact for permanently programming the .mcs file to the flash memory. Please note that XILINX Impact still can temporarily program the .bit file to some of the Artix FPGAs.

Download the latest "Vivado Lab Solutions" from https://www.xilinx.com/support/download.html.

Open "Hardware Manager" in XILINX Vivado. Click on "Open Target" -> "Auto Connect". The software should connect to the FPGA and show it in the "Hardware" section:



To temporarily load a .bit file to the FPGA, right-click the FPGA (xc7a200t) and select "Program Device...":

À Program Device		×
Select a bitstream prog select a debug probes programming file.	ramming file and download it to your hardware device. You can optionally file that corresponds to the debug cores contained in the bitstream	4
Bitstre <u>a</u> m file:	.ware/Bitfiles_A7/EPS/eps1000_PCB60_v1227ARDTRK_f16_r367.bit	•••
Debug probes file:		••••
✓ Enable end of st	tartup check	
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Select the desired .bit file and click "Program". Done!

To permanently store the .mcs file in the flash memory, right-click on the FPGA again and select "Add Configuration Memory Device...". Select "mx25l12872f-spi-x1_x2_x4" (LU1000 devices only) or "s25fl128l" (all other devices):

iect com	guration memory Part			
Search:	Q- s25fl128l		🛞 (1 match)	
Name		Part	Manufact	Alias
🦻 s25f	1281-spi-x1_x2_x4	s25fl128l	Spansion	

Select the desired .mcs-file and click "OK":

Program Configuration Memory Device X					
Select a configuration file and set programming options.					
Memory Device: @ s25fl128l-spi-x1_x2_x4					
Configuration file: 1000_PCB60_v1227ARDTRK_f16_r367.mcs 😒 ····					
PRM file:					
State of non-config mem I/O pins: Pull-none 🗸					
Program Operations					
Address Range: Configuration File Only 🗸					
✓ Erase					
Blank Check					
✓ Program					
✓ Verify					
Verify <u>C</u> hecksum					
SVF Options					
Create SVF Only (no program operations)					
SVF File:					
OK Cancel Apply					

After the flash programming process finished, the FPGA is not programmed yet! To load the program the FPGA you can either unplug the JTAG cable from the instrument and toggle the instrument's power, or right-click on the FPGA in the Vivado software and select "Boot from Configuration Memory Device".