Novoptel

Firmware Update using XILINX Impact

Revision history

Version	Date	Remarks	Author
0.9.0	02.08.2016	Draft version	B. Koch

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Summary

This document describes the firmware update of Novoptel instruments using XILINX Platform Cable USB II and XILINX Impact.

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I. Connect the XILINX programmer to the PC



Fig. 1: XILINX Platform Cable USB II

Use a USB cable to connect the programmer box to the PC. Windows should automatically detect the hardware and install the driver.

II. Verify the XILINX cable driver

If the driver is installed correctly, the LED on the programmer box will glow in orange color. The programmer device should appear in the Windows device manager.



Fig. 2: Windows device manager

The driver version can be verified in the device properties.

III. Connect the XILINX programmer to the Novoptel device

Use the flat ribbon cable to connect the XILINX programmer to the JTAG socket at the rear side of the Novoptel device. Power the Novoptel device. If the connection is correct, the LED on the programmer box will glow in color green as soon as the Novoptel device is powered.

IV. Open XILINX Impact

If the programmer box is connected to a powered Novoptel device, XILINX Impact should be able to automatically detect the programmer.

Cable Communication Setup

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	Communication Mode	
	Parallel Cable III Parallel Cable IV	Platform Cable USB/II Digilent USB JTAG Cable
St SE IMPACT (0.87xd) - E/Xilinx13.4\LabTools\LabTools\auto_project.ipf - [Boundary Scan]		Advanced USB Cable Setup
Image: Second Participation Souther Participation Image: Second Participation Image: Second Participation <	Port: Tr Not Named/000013B3ADEA01 C	CK Speed/Baud Rate:
⊕ ## Boundary Scan Cable Reset ▲ SystemACE Advanced USB Cable Setup ▲ Create PROM F Cable Disconnect ₩ ₩ WebTalk Data	Cable Location O Local Remote Host Name:	
MPACT Proc ++ □ ₽ X Available Operations : A Drogram sElSE R	Cable Plug-in Cable Plug-in. Select or ent xilinx_platformusb PORT=USB21 FR	er a Plug-in from the list below:
	OK Cano	el Help

Fig. 3: Cable setup in XILINX Impact

Create a new project in XILINX Impact. If the programmer is not detected by XILINX Impact, check the configuration setup by opening the "Cable Setup..." in the menu bar. If the programmer is detected, Impact should automatically initialize the JTAG chain. If not, select "File"->"Initialize Chain" in the menu bar.

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IMPACT Flows ↔	MPACT Flows ↔ □ ₽ ×				
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xc6sk100 xcf32p MPACT Proc ↔ □ 5 X bypass bypass	xc6 WDACT free the I I X				
Available Operations : A Program #USE Regist Set #USE Control Set #USE Control	by Act INC				
Vill Boundary Scan	Set Programming Properties				
Console ↔ □ ♬ X	Set Erase Properties				
	::MPACT:1777 - Ling E:/Xilinx/13.4/LabTools/LabTools/spartan6/data/xc6slx100.bsd Console U INFO:IMFACT:1777 - Reading E:/Xilinx/13.4/LabTools/LabTools/spartan6/data/xc6slx100.bsd U INFO:IMFACT:501 - '1': Added Device xc6slx100 successfully. U INFO:IMFACT:501 - '1': Added Device xc6slx100 successfully.				
♥ INFO:IMPACT - Failed to open file: File ?, replace with 'bypass'. ♥ INFO:IMPACT:1777 - Reading E:/Xilinx/13.4/LabTools/LabTools/xcfp/data/xcf32p.bsd ♥ INFO:IMPACT:501 - '2': Added Device xcf32p successfully.	<pre>UINFO:IMFACT - Failed to open file: File ?, replace with 'bypass'. UINFO:IMFACT:1777 - Reading E:/Kilinx/13.4/LabTools/LabTools/xcfp/data/xcf32p.bsd UINFO:IMFACT:501 - '2': Added Device xcf32p successfully.</pre>				
Configuration Platform Cable USB II 6 MHz Usb-hs	Conside 👽 errors 🔔 Warnings				

Fig. 4: Correct JTAG chain in XILINX Impact

If the JTAG chain is initialized correctly, two devices should be accessible. An FPGA (e.g. xc6sxl100) and a flash memory (e.g. xcf32p). The FPGA can be programmed using a .bit file to test new firmwares without overwriting the old one until you cycle the power. The flash memory can be programmed with a .mcs file to permanently upgrade the firmware. The .bit and .mcs files are provided by Novoptel upon request. Right-click on a device and select "Assign New Configuration File..." to assign a file.

- Boundary-Scan - Device 1 (EPGA xc6sly100.)	Property Name	Value
Device 2 (PROM2 xcf32p)	Verify	
	General CPLD And PROM Properties	
	Design-Specific Erase Before Programming	
	Read Protect	
	PROM/CoolRunner-II Usercode (8 Hex Digits)	
	PROM Specific Properties	
	Load FPGA	
	Parallel Mode	
	Advanced PROM Programming Properties	
	During Configuration: PROM is Configuration Master	
	[select clock source]	External Clock 👻
	During Configuration: PROM is Slave (clocked extern	
	During Configuration: PROM is Configuration Master [select clock source] During Configuration: PROM is Slave (clocked extern	External Clock

Fig. 5: Programming properties

Before programming the .mcs file, verify the programming properties. Right-click on the flash memory and select "Set Programming Properties…". It is important that the menu item "Design-Specific Erase Before Programming" is activated, see Fig. 5. Finally the programming is started by right-clicking the device and selecting "Program".